

What Is Claimed Is:

1 1. A charged-device model (CDM) electrostatic discharge
2 (ESD) protection circuit for an integrated circuit (IC), the
3 ESD protection circuit comprising:

4 an ESD clamp device, coupled to a pad and a substrate
5 having a first conductivity type, the ESD clamp device being
6 closed under normal power operation; and

7 a functional component, formed on the substrate and
8 coupled to the pad, the functional component having a first
9 well of the first conductivity type and an isolating region
10 of a second conductivity type, the second conductivity type
11 being the reversed polarity of the first conductivity type,
12 and the isolating region isolating the first well from the
13 substrate; the functional component transmitting signals
14 between the IC and an external linkage under normal power
15 operation.

1 2. The CDM ESD protection circuit in claim 1, wherein when
2 the isolating region comprises a second well surrounding the
3 first well and a deep well under the first well.

1 3. The CDM ESD protection circuit in claim 1, wherein the
2 isolating region is coupled to a first power supply and the
3 first well is coupled to a second power supply.

1 4. The CDM ESD protection circuit in claim 1, wherein the
2 functional component comprises a metal-oxide semiconductor
3 (MOS) having the second conductivity type in the first well.

1 5. The CDM ESD protection circuit in claim 1, wherein the
2 ESD clamp device comprises an MOS diode having two ends
3 respectively coupled to the pad and the substrate.

1 6. The CDM ESD protection circuit in claim 1, wherein the
2 ESD clamp device is a two-stage ESD protection circuit,
3 having a primary ESD protection circuit coupled between the
4 pad and the substrate, a secondary ESD protection circuit
5 coupled between the functional component and the substrate,
6 and a resistor coupled between the functional component and
7 the pad.

1 7. The CDM ESD protection circuit in claim 1, wherein the
2 first conductivity type is an N type, and the second
3 conductivity type is p type.

1 8. The CDM ESD protection circuit in claim 1, wherein the
2 first conductivity type is a p type, and the second
3 conductivity type is N type.

1 9. A charged-device model (CDM) electrostatic discharge
2 (ESD) protection circuit for an input port of an integrated
3 circuit (IC), the ESD protection circuit comprising:

4 an ESD clamp device, coupled to a pad and a substrate
5 having a first conductivity type, under normal power
6 operation, the ESD clamp device being closed; and

7 an MOS component having a second conductivity type,
8 formed in a first well on the substrate and coupled to the
9 pad; an isolating region having the second conductivity type
10 being formed between the first well and the substrate to
11 separate the first well and the substrate, the second
12 conductivity type being the reversed polarity of the first
13 conductive type, and under normal power operation, the MOS
14 component transmitting signals from the pad into the IC.

1 10. The CDM ESD protection circuit in claim 9, wherein a
2 gate of the MOS component is coupled to the pad.

1 11. The CDM ESD protection circuit in claim 9, wherein the
2 source of the MOS component is coupled to an internal power
3 line.

1 12. The CDM ESD protection circuit in claim 11, wherein the
2 CDM ESD protection circuit further comprises an ESD
3 protection circuit coupled between the gate of the MOS
4 component and the internal power line.

1 13. The CDM ESD protection circuit in claim 12, wherein the
2 ESD protection circuit at the input port is an gate-grounded
3 MOS component.

1 14. The CDM ESD protection circuit in claim 11, wherein the
2 first well is coupled to the internal power line.

1 15. A charged-device model (CDM) electrostatic discharge
2 (ESD) protection circuit for an output port of an integrated
3 circuit (IC), the ESD protection circuit comprising:

4 an ESD clamp device, coupled to a pad and a substrate
5 having the first conductivity type, under normal power
6 operation, the ESD clamp device being closed; and

7 an MOS component having a second conductivity type,
8 formed in a first well on the substrate and coupled to the
9 pad; an isolating region having the second conductivity type
10 being formed between the first well and the substrate to
11 separate the first well and the substrate, the second
12 conductivity type being the reversed polarity of the first
13 conductive type, and under normal power operation, the MOS
14 component transmitting signals from the IC to the pad.

1 16. The CDM ESD protection circuit in claim 15, wherein a
2 drain of the MOS component is coupled to the pad, a source
3 of the MOS component and the first well are coupled to an
4 I/O power line.

1 17. The CDM ESD protection circuit in claim 15, wherein a
2 plurality of diodes are disposed between the I/O power line
3 and an internal power line.

1 18. A CDM ESD protection circuit, suitable for an I/O port
2 of a high voltage IC, the CDM ESD protection circuit
3 comprises:

4 an ESD clamp device, coupled between a pad and a p-type
5 substrate, the ESD clamp device being closed under normal
6 power operation; and

7 a first NMOS (N-type metal-on-semiconductor) component
8 formed on a P-type first isolated well on the substrate, an
9 N-type isolating region being formed to separate the P-type
10 first isolated well and the substrate; the NMOS component
11 having a gate coupled to a high power line, a first
12 source/drain coupled the pad, and a second source/drain
13 coupled to an input buffer; and

14 an output driver comprising a second and a third NMOS
15 component respectively formed in a P-type second isolated
16 well on the substrate and connected in series; an N-type
17 second isolating region formed between the P-type second
18 isolated well and the substrate, a gate of the second NMOS
19 component, coupled to the high Power line, a drain of the
20 second NMOS component coupled to the pad, a source of the
21 second NMOS component coupled to a drain of the third NMOS
22 component, a source of the third NMOS component coupled to
23 an I/O low power line, and a gate of the third NMOS
24 component being to a pre-output driver.

1 19. The CDM ESD protection circuit in claim 18, wherein the
2 first isolated well is coupled to an internal low power
3 line, the second isolated well is coupled to the I/O low
4 power line.

1 20. The CDM ESD protection circuit in claim 19, wherein a
2 plurality of diodes are disposed between the internal low
3 power line and the I/O low power line.

1 21. The CDM ESD protection circuit in claim 18, wherein the
2 ESD clamp device comprises a forth NMOS component and a
3 fifth NMOS component, connected in series between the pad
4 and I/O low power line, a gate of the forth NMOS component
5 is coupled to the high power line, and a gate of the fifth
6 NMOS component is coupled to the I/O low power line.

22. The CDM ESD protection circuit in claim 18, wherein an
ESD protection resistor is formed between the first NMOS
component and the pad.